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| 10/633,055 | 07/31/2003 | Shahriar Ahmed | 42P10970C | 3607 |

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| EXAMINER | |
|---|---|
| IM, JUNGHWA M | |

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**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 10/633,055 | AHMED ET AL. | |
| | Examiner | Art Unit | |
| | Junghwa M. Im | 2811 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *23 August 2007*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *13,17-22 and 27-31* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☐ Claim(s) _____ is/are rejected.

7)☒ Claim(s) *13,17-22 and 27-31* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

## DETAILED ACTION

### *Double Patenting*

The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970);and, *In re Thorington,* 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claims 1-4, 6-9, 11-14, 16-19, 21-24, 26-29 and 31-34 are rejected on the ground of nonstatutory obviousness-type double patenting as being unpatentable over claims 1-40 of U.S. Patent No. 6,703,685 in view of U.S. Patent No. 4,982,257 to Akbar et al. (Akcar).

The conflicting claims are substantially identical in structure and material wise. In a comparison of pending claim 13, for example, and claim 10 of '685 patent, the substantial difference is that pending claim 13 requires a limitation of "an emitter cut provided at the bottom of said emitter stack and on top of an intrinsic base structure formed in the substrate." However, Fig. 8 of Akbar shows an emitter cut (an emitter/base junction) provided at the bottom of said emitter stack and on top of an intrinsic base structure (a portion of the base in contact with the emitter) formed in the substrate.

It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Akbar to the device of '239 patent in order to have an emitter cut

provided at the bottom of said emitter stack and on top of an intrinsic base structure formed in the substrate to reduce the device size.

Claims 17, 27 and 31 are substantially identical to claims 11, 13 and 14 of '685 patent.

Regarding claim 18, Fig. 8 of Akbar shows a bipolar junction transistor further including:

a collector structure 12 disposed in the substrate below the emitter stack; and

an intrinsic base structure 14 disposed between the emitter stack 16 and the collector structure 12.

Regarding claim 19, Fig. 8 of Akbar shows a bipolar junction transistor further including:

a collector structure 12 disposed in the substrate below the emitter stack; and

a dielectric layer 18, 20 disposed above the substrate and below the emitter stack and above the collector structure; and

an intrinsic base structure 14 disposed between the emitter stack and the collector structure.

Fig. 8 of Akbar shows most aspect of the instant invention except "the dielectric layer is patterned for said emitter cut to be formed therein." Fig. 9 of Harame shows a semiconductor device wherein the dielectric layer 34, 36 is patterned for the emitter cut (a bottom portion of the emitter 40) to be formed therein. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Harame into the device of Akbar in order to have to a semiconductor device wherein the dielectric layer patterned for the emitter cut to reduce parasite capacitance between the emitter and the extrinsic base.

Regarding claim 20, Fig. 8 of Akbar shows a collector tap 26 is N type.

Regarding claim 21, Akbar discloses that the substrate includes a BiCMOS structure (col. 1, lines 11-14).

Regarding claim 22, Fig. 8 of Akbar shows the BJT is selected from a monojunction BJT device and a heterojunction BJT device.

Regarding claim 28, Fig. 8 of Akbar shows the bipolar junction transistor is an NPN transistor, and the collector tap is N type.

Regarding claim 29, Akbar discloses the bipolar junction transistor is an PNP transistor, and the collector tap is P type (col. 3, lines 24-25).

Regarding claim 30, Fig. 8 of Akbar shows the collector tap has no doping that is different from the substrate.

***Claim Rejections - 35 USC § 103***

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 13, 17-22 and 27-31 are rejected under 35 U.S.C. 103(a) as being unpatentable over Akbar et al. (U.S. Pat. No. 4957875), hereinafter Akbar in view of Eklund (U.S. Pat. No. 5087580).

Regarding claim 13, Fig. 8 of Akbar shows a bipolar junction transistor comprising:

in a substrate 32, a first isolation structure 36 spaced apart from a second isolation structure 38;

an epitaxial base layer 14 formed in the substrate;

an emitter stack 16 disposed above the substrate and between the first isolation structure and the second isolation structure wherein the emitter stack had an emitter stack perimeter;

a recess (a portion between the regions 17, 18) disposed immediately adjacent to the emitter stack and disposed between the emitter stack and the first isolation structure, wherein the recess exposes a collector tap 30 collector tap having a collector tap perimeter , wherein the emitter stack and the recess share a boundary; and the emitter stack and the collector tap perimeter share a co-boundary (Fig. 9).

Fig. 8 of Akbar shows most aspect of the instant invention except "an emitter cut provide at the bottom of said emitter stack and on top of an intrinsic base structure formed in the substrate." Fig. 1 of Eklund shows a semiconductor device wherein an emitter cut (a bottom portion 61 of the emitter 60) provide at the bottom of said emitter stack and on top of an intrinsic base structure (a portion labeled 61) formed in the substrate. It would have been obvious to one of ordinary skill in the art at the time of the invention to incorporate the teachings of Eklund into the device of Akbar in order to have an emitter cut provided at the bottom of said emitter stack and on top of an intrinsic base structure in the substrate to reduce parasite capacitance between the emitter and the extrinsic base.

Regarding claim 17, Fig. 8 of Akbar shows a buried layer 34 in the substrate between the first isolation structure and the second isolation structure.

Regarding claim 18, Fig. 8 of Akbar shows a bipolar junction transistor further including:

in a substrate, an epitaxial base layer 14 disposed below the emitter stack;

a collector structure 12 disposed in the substrate below the emitter stack; and

an intrinsic base structure 22 disposed between the emitter stack and the collector structure.

Regarding claim 19, Fig. 8 of Akbar shows a bipolar junction transistor further including:

a collector structure 12 disposed in the substrate below the emitter stack;

a dielectric layer 17 disposed above the substrate and below the emitter stack and above the collector structure; and

an intrinsic base structure 22 disposed between the emitter stack and the collector structure. And Fig. 1 of Eklund shows a semiconductor device wherein the dielectric layer (44, 50, 74) is patterned for the emitter cut to be formed therein. Therefore, the combination of Akbar/Eklund would show that a collector structure disposed in the substrate below the emitter stack; a dielectric layer disposed above the substrate and below the emitter stack and above the collector structure; and an intrinsic base structure disposed between the emitter stack and the collector structure; and wherein the dielectric layer (44, 50, 74) is patterned for the emitter cut to be formed therein.

Regarding claim 20, Fig. 8 of Akbar shows a collector tap 26 is N type.

Regarding claim 21, Fig. 1 of Eklund shows that the substrate includes a BiCMOS structure (col. 3, lines 52-55).

Regarding claim 22, Fig. 8 of Akbar shows the BJT is selected from a monojunction BJT device and a heterojunction BJT device.

Regarding claim 27, Fig. 8 of Akbar shows the collector tap 127 is self-aligned with the emitter stack.

Also, note that "self-aligned" is a process designation and would thus not carry patentable weight in this claim drawn to a product. See *In re Thorp,* 227 USPQ 964 (Fed. Cir. 1985).

Regarding claim 28, Fig. 8 of Akbar shows the bipolar junction transistor is an NPN transistor, and the collector tap is N type.

Regarding claim 29, Akbar discloses the bipolar junction transistor is an PNP transistor, and the collector tap is P type (col. 3, lines 24-25).

Regarding claim 30, Fig. 8 of Akbar shows the collector tap has no doping that is different from the substrate.

Regarding claim 31, Fig. 8 of Akbar shows the recess is a contact corridor.

### *Response to Arguments*

Applicant's arguments with respect to pending claims have been considered but are moot in view of the new ground(s) of rejection.

### *Conclusion*

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Junghwa M. Im whose telephone number is (571) 272-1655. The examiner can normally be reached on MON.-FRI. 8:30AM-5:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Lynne A. Gurley can be reached on (571) 272-1670. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Junghwa M. Im
Examiner
Art Unit 2811

jmi
9/12/2007